EE/CprE/SE 491 WEEKLY REPORT 8

31/10/24 - 7/11/24

sdmay25-16

Project title: Multi-Channel High-Gain Low Noise Amplifier for High-Frequency Ultrasound Signal Acquisition

Client &/Advisor: Manojit Pramanik

Team Members/Role:
Jon Wetenkamp, Yash Gaonkar, Ethan Hulinksy, Ryan Ellerbach

- **Weekly Summary:** This week we the team mainly focused on seeing if we could solve the irregularities between the actual prototype and the simulation we ran in Ni-Multisim. We also tried to see if by changing the biasing voltage the clipping we see on the oscilloscope would go away. After changing the biasing voltage, the clipping seen on the oscilloscope did go down quite a bit, but we saw some very weird values for the output. The reason for that was the second amplifier in the cascading design we have does not seem to affect the output in any way. For this we had two options, one fixes the first design or inputs a second design that works but the values of the capacitors and resistors would have to change. After working on the actual prototype, we were able to get our simulations to match the results of the actual prototype. This allowed us to run some simulations and finalize the resistors we need and capacitors we need to make the gain and output voltage fall in the requirements laid out to us by our design contact. We also had our biweekly meeting with our client Manojit Pramanik.
- **Past week accomplishments** Member 1: Worked on… □ Team Member 2:
    - Yash Gaonkar: Retraced the design for another amplifier circuit and worked on finding capacitor values.
    - Ethan Hulinsky: Worked on the simulation in NI-Multisim and worked on the prototype to see why the second stage was not affecting the output
    - Ryan Ellerbach: Retraced the design for another amplifier circuit and worked on finding capacitor values. Also worked on getting the simulation output to match the prototype output
    - Jon Wetenkamp: Worked on the simulation in NI-Multisim and worked on the prototype to see why the second stage was not affecting the output

  Pending issues

There are no pending issues currently, right now we have ordered some components from digikey and we will see if the values are good. We might get started on some of the EM shielding next week.

Past week accomplishments

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Jonathan Wetenkamp	Worked on the simulation in NI-Multisim and worked on the prototype to see why the second stage was not affecting the output	4	26.5
Yash Gaonkar	Retraced the design for another amplifier circuit and worked on finding capacitor values.	4	24.5
Ryan Ellerbach	Retraced the design for another amplifier circuit and worked on finding capacitor values. Also worked on getting the simulation output to match the prototype output	4	28.5
Ethan Hulinsky	Worked on the simulation in NI-Multisim and worked on the prototype to see why the second stage was not affecting the output	4	32

- **Plans for the upcoming week**

As mentioned above we have ordered components from digikey and we will see if the values we have obtained from running simulations will work with our design. We might also get started on the EM shielding components of the project.